

## TLVx316

# 10MHz、轨到轨输入/输出、低电压、1.8V CMOS 运算放大器

### 1 特性

- 单位增益带宽：10MHz
- 低  $I_Q$ ：每通道 400 $\mu$ A
  - 出色的功率带宽比
  - 在温度和电源电压范围内保持稳定的  $I_Q$
- 宽电源电压范围：1.8V 至 5.5V
- 低噪声：1kHz 时为 12nV/ $\sqrt{\text{Hz}}$
- 低输入偏置电流： $\pm 10$ pA
- 偏移电压： $\pm 0.75$ mV
- 单位增益稳定
- 内部射频干扰 (RFI)/电磁干扰 (EMI) 滤波器
- 扩展温度范围： $-40^\circ\text{C}$  至  $+125^\circ\text{C}$

### 2 应用范围

- 电池供电仪器：
  - 消费类应用、工业应用、医疗应用
  - 笔记本电脑、便携式媒体播放器
- 传感器信号调节
- 条形码扫描器
- 有源滤波器
- 音频

### 3 说明

TLV316（单路）、TLV2316（双路）和 TLV4316（四路）器件构成了低功耗、通用运算放大器系列。该系列器件 特有轨到轨输入和输出摆幅，并且兼具低静态电流（每通道的典型值为 400 $\mu$ A）、10MHz 的较宽带宽和超低噪声（1kHz 时为 12 nV/ $\sqrt{\text{Hz}}$ ），因此对于要求在成本和性能间达到良好平衡的各类电池供电应用而言极具吸引力。低输入偏置电流支持在源阻抗高达兆欧级的应用中使用此类运算放大器。

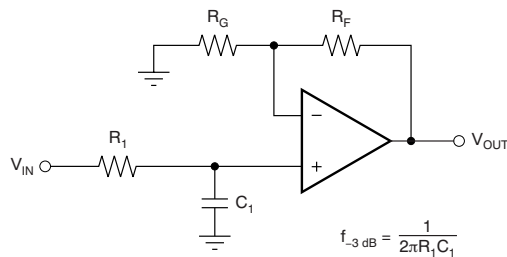
TLVx316 采用稳健耐用的设计，方便电路设计人员使用。该器件具有单位增益稳定的集成 RFI/EMI 抑制滤波器，在过驱条件下不会出现反相，并且具有高静电放电 (ESD) 保护 (4kV HBM)。

此类器件经过优化，适合在 1.8V ( $\pm 0.9$ V) 至 5.5V ( $\pm 2.75$ V) 的低电压状态下工作。这些最新补充的低电压互补金属氧化物半导体 (CMOS) 运算放大器与 TLVx313 和 TLVx314 系列搭配，为用户提供了广泛的带宽、噪声和功率选择，可以满足各种应用的需求。

器件信息<sup>(1)</sup>

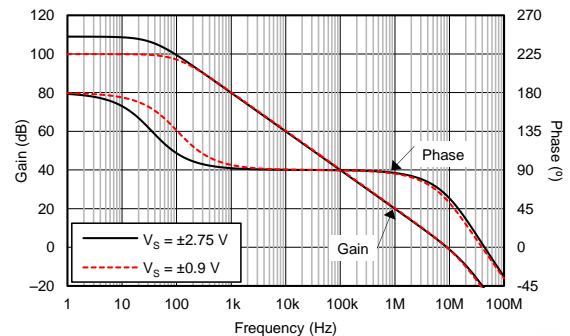
器件型号	封装	封装尺寸 (标称值)
TLV316	SC70 (5)	1.25mm x 2.00mm
	SOT-23 (5)	1.60mm x 2.90mm
TLV2316	VSSOP (8)	3.00mm x 3.00mm
	SOIC (8)	3.91mm x 4.90mm
TLV4316	TSSOP (14)	4.40mm x 5.00mm
	SOIC (14)	8.65mm x 3.91mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

单极低通滤波器



10MHz 带宽下的低电源电流 (400 $\mu$ A/通道)



## 目录

<b>1</b>	特性 .....	1	8.3	Feature Description .....	14
<b>2</b>	应用范围 .....	1	8.4	Device Functional Modes .....	15
<b>3</b>	说明 .....	1	<b>9</b>	<b>Application and Implementation</b> .....	16
<b>4</b>	修订历史记录 .....	2	9.1	Application Information .....	16
<b>5</b>	<b>Device Comparison Table</b> .....	3	9.2	System Examples .....	16
<b>6</b>	<b>Pin Configuration and Functions</b> .....	3	<b>10</b>	<b>Power Supply Recommendations</b> .....	17
<b>7</b>	<b>Specifications</b> .....	6	10.1	Input and ESD Protection .....	17
7.1	Absolute Maximum Ratings .....	6	<b>11</b>	<b>Layout</b> .....	18
7.2	ESD Ratings .....	6	11.1	Layout Guidelines .....	18
7.3	Recommended Operating Conditions .....	6	11.2	Layout Example .....	18
7.4	Thermal Information: TLV316 .....	7	<b>12</b>	器件和文档支持 .....	19
7.5	Thermal Information: TLV2316 .....	7	12.1	文档支持 .....	19
7.6	Thermal Information: TLV4316 .....	7	12.2	相关链接 .....	19
7.7	Electrical Characteristics .....	8	12.3	社区资源 .....	19
7.8	Typical Characteristics .....	9	12.4	商标 .....	19
7.9	Typical Characteristics .....	10	12.5	静电放电警告 .....	20
<b>8</b>	<b>Detailed Description</b> .....	13	12.6	Glossary .....	20
8.1	Overview .....	13	<b>13</b>	机械、封装和可订购信息 .....	20
8.2	Functional Block Diagram .....	13			

## 4 修订历史记录

### Changes from Original (February 2016) to Revision A

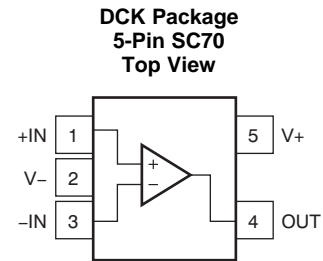
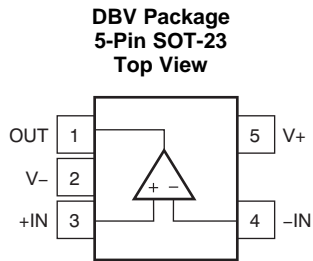
**Page**

•	已添加 14 引脚 SOIC 封装信息至器件信息表 .....	1
•	Added D package to PW package pinout drawing .....	5
•	Added D (SOIC) thermal values to <i>Thermal Information: TLV4316</i> table .....	7

## 5 Device Comparison Table

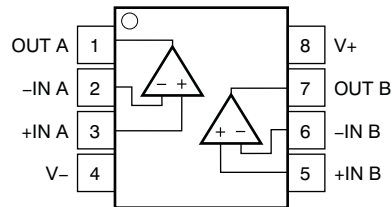
DEVICE	NO. OF CHANNELS	PACKAGE-LEADS				
		DBV	DCK	D	DGK	PW
TLV316	1	5	5	—	—	—
TLV2316	2	—	—	8	8	—
TLV4316	4	—	—	14	—	14

## 6 Pin Configuration and Functions



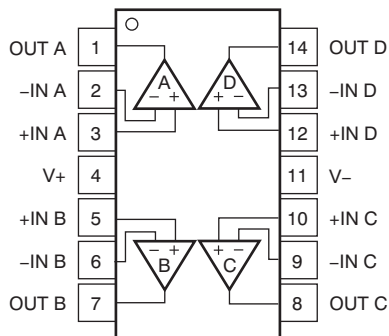
### Pin Functions: TLV316

NAME	PIN		I/O	DESCRIPTION
	DBV (SOT-23)	DCK (SC70)		
-IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V-	2	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

**D, DGK Packages  
8-Pin SOIC, VSSOP  
Top View**

**Pin Functions: TLV2316**

PIN		I/O	DESCRIPTION
NO.	NAME		
2	-IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
6	-IN B	I	Inverting input, channel B
5	+IN B	I	Noninverting input, channel B
1	OUT A	O	Output, channel A
7	OUT B	O	Output, channel B
4	V-	—	Negative (lowest) supply or ground (for single-supply operation)
8	V+	—	Positive (highest) supply

**D, PW Packages  
14-Pin SOIC, TSSOP  
Top View**



**Pin Functions: TLV4316**

PIN		I/O	DESCRIPTION
NO.	NAME		
2	-IN A	I	Inverting input, channel A
3	+IN A	I	Noninverting input, channel A
6	-IN B	I	Inverting input, channel B
5	+IN B	I	Noninverting input, channel B
9	-IN C	I	Inverting input, channel C
10	+IN C	I	Noninverting input, channel C
13	-IN D	I	Inverting input, channel D
12	+IN D	I	Noninverting input, channel D
1	OUT A	O	Output, channel A
7	OUT B	O	Output, channel B
8	OUT C	O	Output, channel C
14	OUT D	O	Output, channel D
11	V-	—	Negative (lowest) supply or ground (for single-supply operation)
4	V+	—	Positive (highest) supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage			7		V
Signal input pins	Voltage <sup>(2)</sup>	Common-mode	(V <sub>-</sub> ) - 0.5	(V <sub>+</sub> ) + 0.5	V
		Differential	(V <sub>+</sub> ) - (V <sub>-</sub> ) + 0.2		
	Current <sup>(2)</sup>	-10	10	mA	
Output short-circuit <sup>(3)</sup>			Continuous		mA
Temperature	Specified, T <sub>A</sub>		-40	125	°C
	Junction, T <sub>J</sub>		150		
	Storage, T <sub>stg</sub>		-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>S</sub>	Supply voltage	1.8		5.5	V
Specified temperature range		-40		125	°C

## 7.4 Thermal Information: TLV316

THERMAL METRIC <sup>(1)</sup>		TLV316		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51.0	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	26.1	1.0	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	49.0	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 7.5 Thermal Information: TLV2316

THERMAL METRIC <sup>(1)</sup>		TLV2316		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.2	186.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.6	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.2	107.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	22.0	15.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	67.6	106.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 7.6 Thermal Information: TLV4316

THERMAL METRIC <sup>(1)</sup>		TLV4316		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.2	87.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.2	44.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	41.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	4.9	11.6	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	58.3	41.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 7.7 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted);  $V_S$  (total supply voltage) =  $(V+) - (V-) = 1.8\text{ V to } 5.5\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V}$		$\pm 0.75$	$\pm 3$	mV
		$V_S = 5\text{ V}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$			$\pm 4.5$	
$dV_{OS}/dT$	Drift	$V_S = 5\text{ V}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$		$\pm 2$		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 1.8\text{ V} - 5.5\text{ V}$ , $V_{CM} = (V-)$		$\pm 30$	$\pm 175$	$\mu\text{V}/\text{V}$
	Channel separation, dc	At dc		100		dB
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$V_S = 5.5\text{ V}$	$(V-) - 0.2$		$(V+) + 0.2$	V
CMRR	Common-mode rejection ratio	$V_S = 5.5\text{ V}$ , $(V-) - 0.2\text{ V} < V_{CM} < (V+) - 1.4\text{ V}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$	72	90		dB
		$V_S = 5.5\text{ V}$ , $V_{CM} = -0.2\text{ V to } 5.7\text{ V}$ , $T_A = -40^\circ\text{C to } +125^\circ\text{C}$		75		
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			$\pm 10$		pA
$I_{OS}$	Input offset current			$\pm 10$		pA
<b>NOISE</b>						
$E_n$	Input voltage noise (peak-to-peak)	$V_S = 5\text{ V}$ , $f = 0.1\text{ Hz to } 10\text{ Hz}$		5		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$V_S = 5\text{ V}$ , $f = 1\text{ kHz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input current noise density	$f = 1\text{ kHz}$		1.3		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT IMPEDANCE</b>						
$Z_{ID}$	Differential			$2 \parallel 2$		$10^{16}\Omega \parallel \text{pF}$
$Z_{IC}$	Common-mode			$2 \parallel 4$		$10^{11}\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$V_S = 5.5\text{ V}$ , $(V-) + 0.05\text{ V} < V_O < (V+) - 0.05\text{ V}$ , $R_L = 10\text{ k}\Omega$	100	104		dB
		$V_S = 5.5\text{ V}$ , $(V-) + 0.15\text{ V} < V_O < (V+) - 0.15\text{ V}$ , $R_L = 2\text{ k}\Omega$		104		
<b>FREQUENCY RESPONSE</b>						
GBP	Gain bandwidth product	$V_S = 5\text{ V}$ , $G = +1$		10		MHz
$\phi_m$	Phase margin	$V_S = 5\text{ V}$ , $G = +1$		60		Degrees
SR	Slew rate	$V_S = 5\text{ V}$ , $G = +1$		6		$\text{V}/\mu\text{s}$
$t_S$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V step, $G = +1$ , $C_L = 100\text{ pF}$		1		$\mu\text{s}$
$t_{OR}$	Overload recovery time	$V_S = 5\text{ V}$ , $V_{IN} \times \text{gain} = V_S$		0.8		$\mu\text{s}$
THD + N	Total harmonic distortion + noise <sup>(1)</sup>	$V_S = 5\text{ V}$ , $V_O = 0.5 V_{RMS}$ , $G = +1$ , $f = 1\text{ kHz}$		0.008%		
<b>OUTPUT</b>						
$V_O$	Voltage output swing from supply rails	$V_S = 1.8\text{ V to } 5.5\text{ V}$ , $R_L = 10\text{ k}\Omega$ ,			35	mV
		$V_S = 1.8\text{ to } 5.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ ,			125	
$I_{SC}$	Short-circuit current	$V_S = 5\text{ V}$		$\pm 50$		mA
$Z_O$	Open-loop output impedance	$V_S = 5\text{ V}$ , $f = 10\text{ MHz}$		250		$\Omega$
<b>POWER SUPPLY</b>						
$V_S$	Specified voltage range		1.8		5.5	V
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}$ , $I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C to } 125^\circ\text{C}$		400	575	$\mu\text{A}$
<b>TEMPERATURE</b>						
$T_A$	Specified		-40		125	$^\circ\text{C}$
$T_{stg}$	Storage		-65		150	$^\circ\text{C}$

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.



## 7.8 Typical Characteristics

**Table 1. Table of Graphs**

TITLE	FIGURE
Offset Voltage Production Distribution	<a href="#">Figure 1</a>
Offset Voltage vs Common-Mode Voltage	<a href="#">Figure 2</a>
Open- Loop Gain and Phase vs Frequency	<a href="#">Figure 3</a>
Input Bias and Offset Current vs Temperature	<a href="#">Figure 4</a>
Input Voltage Noise Spectral Density vs Frequency	<a href="#">Figure 5</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 6</a>
Small-Signal Overshoot vs Load Capacitance	<a href="#">Figure 7</a>
No Phase Reversal	<a href="#">Figure 8</a>
Small-Signal Step Response	<a href="#">Figure 9</a>
Large-Signal Step Response	<a href="#">Figure 10</a>
Short-Circuit Current vs Temperature	<a href="#">Figure 11</a>
Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency	<a href="#">Figure 12</a>
Channel Separation vs Frequency	<a href="#">Figure 13</a>

### 7.9 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

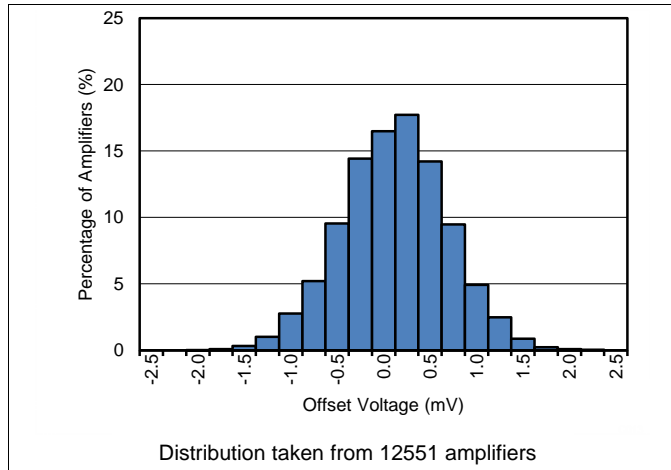


Figure 1. Offset Voltage Production Distribution

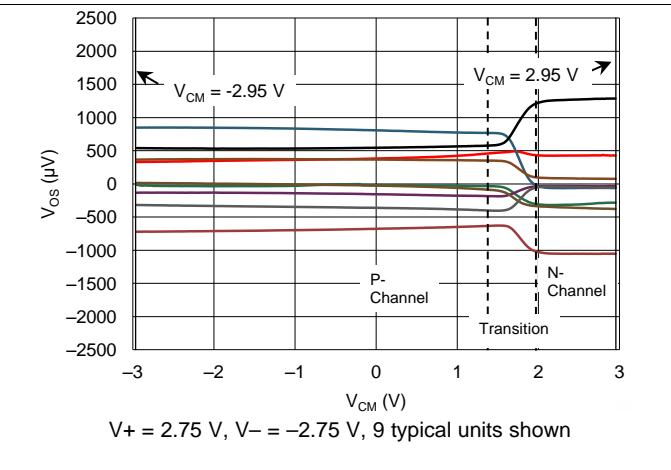


Figure 2. Offset Voltage vs Common-Mode Voltage

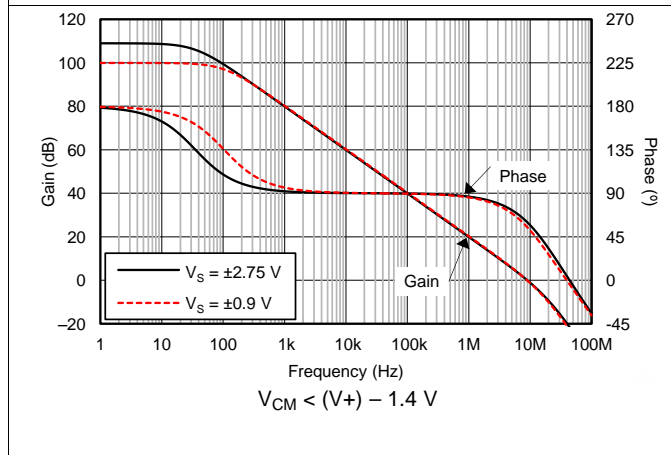


Figure 3. Open-Loop Gain and Phase vs Frequency

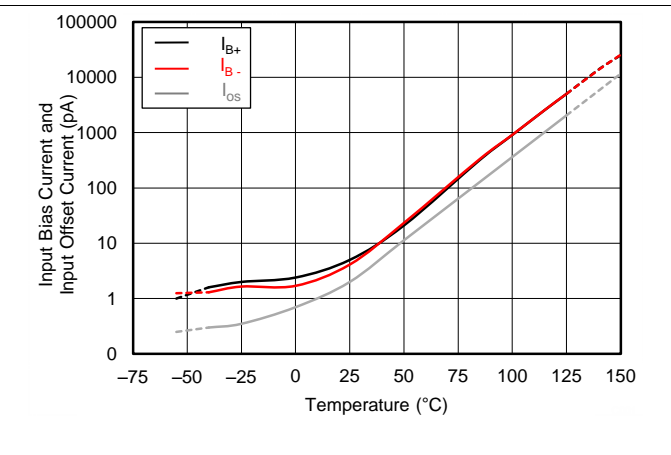


Figure 4. Input Bias and Offset Current vs Temperature

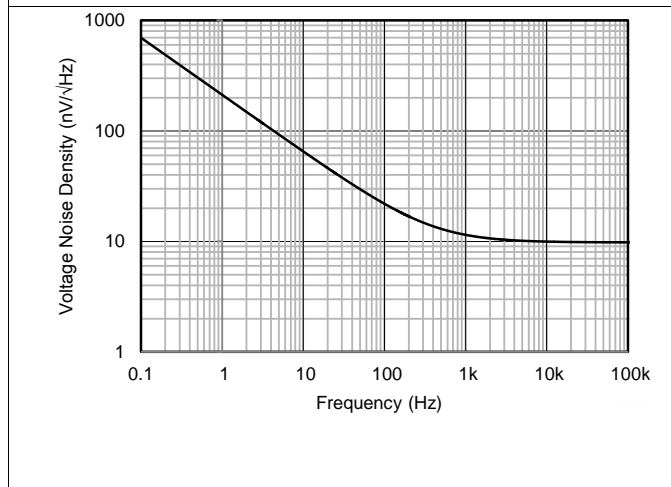


Figure 5. Input Voltage Noise Spectral Density vs Frequency

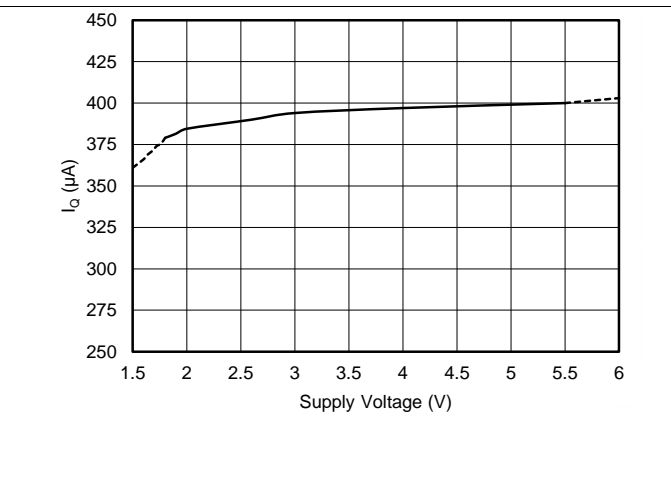


Figure 6. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

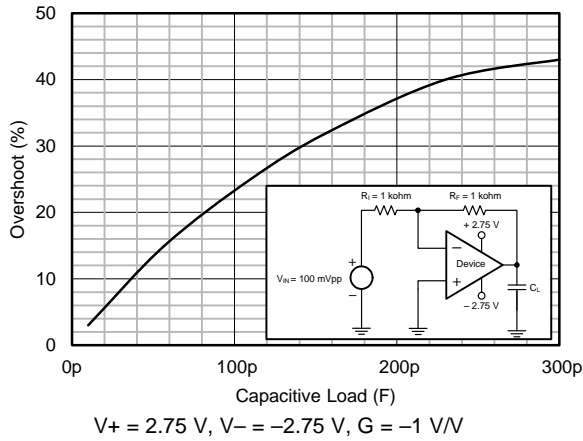


Figure 7. Small-Signal Overshoot vs Load Capacitance

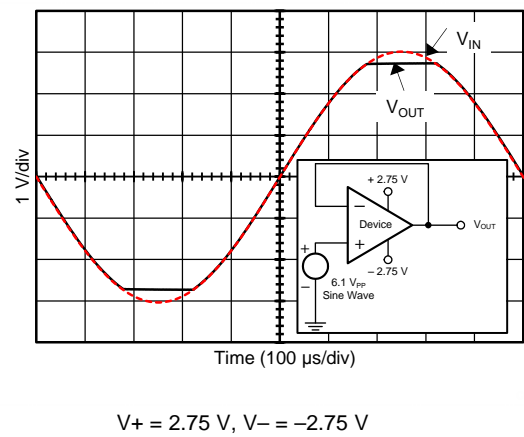


Figure 8. No Phase Reversal

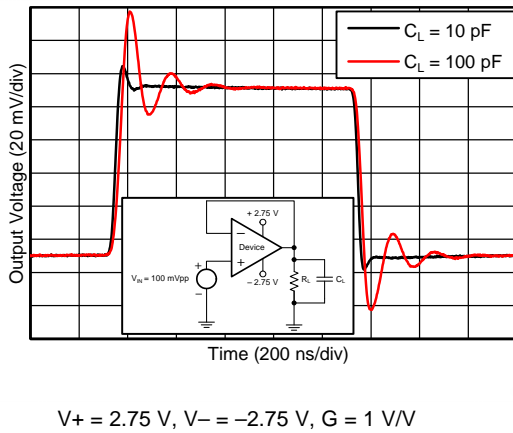


Figure 9. Small-Signal Step Response

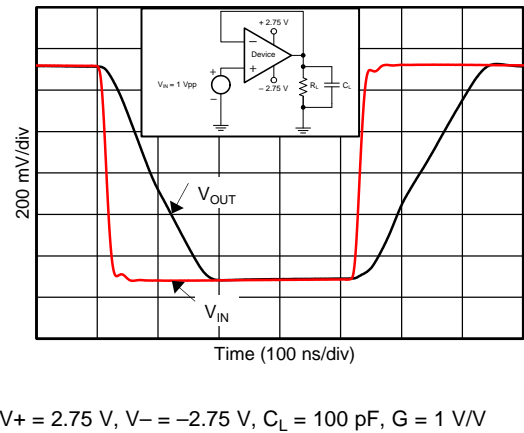


Figure 10. Large-Signal Step Response

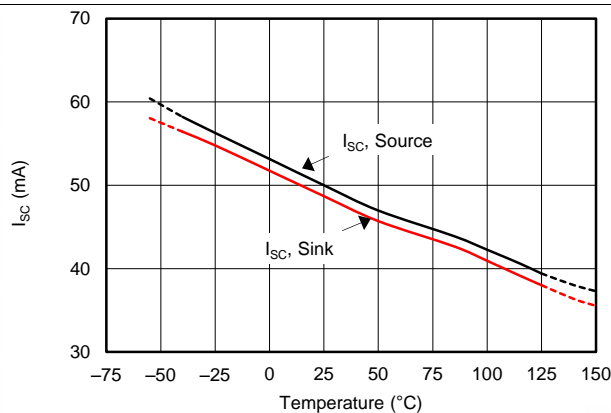


Figure 11. Short-Circuit Current vs Temperature

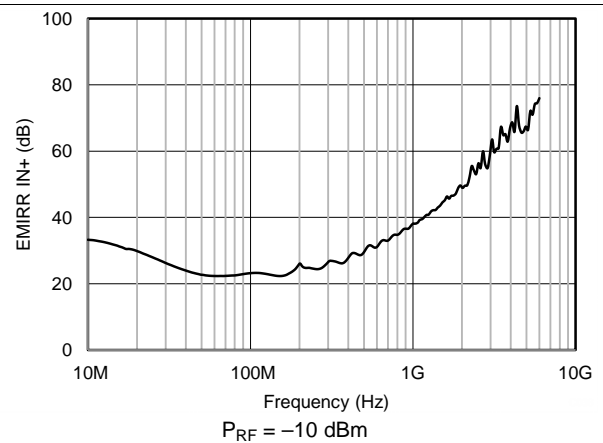
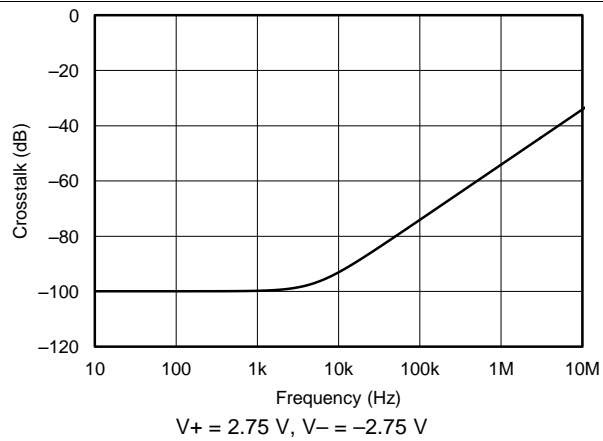


Figure 12. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency

**Typical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



**Figure 13. Channel Separation vs Frequency**

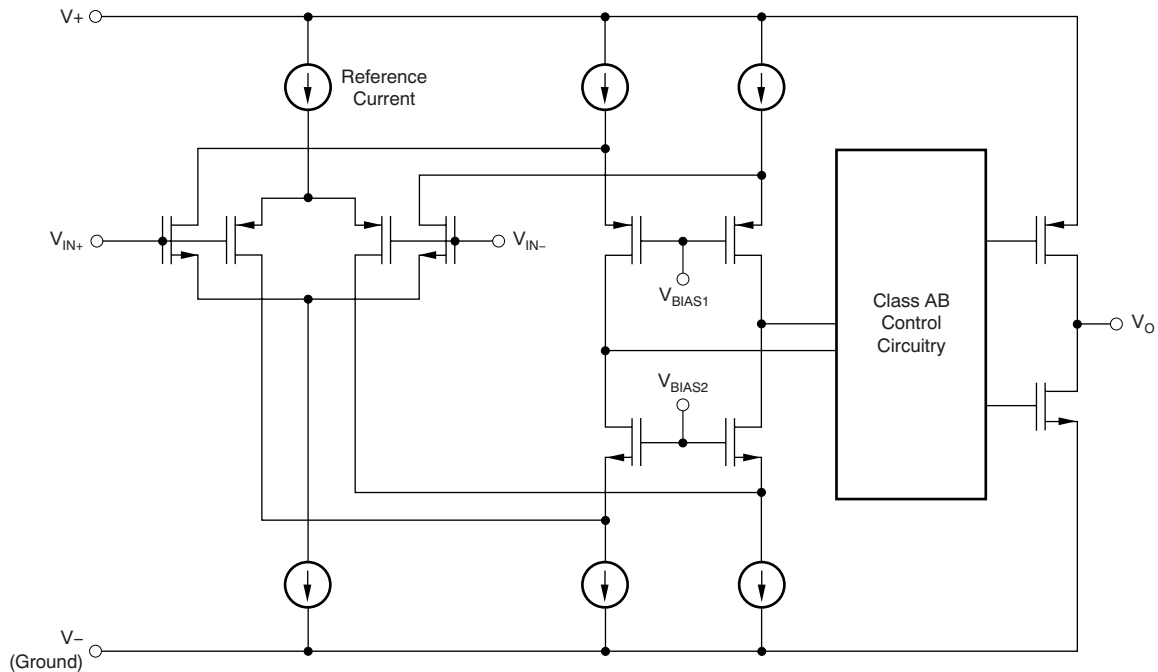
## 8 Detailed Description

### 8.1 Overview

The TLVx316 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving  $\leq 10\text{-k}\Omega$  loads connected to any point between  $V_+$  and ground. The input common-mode voltage range includes both rails and allows the TLVx316 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx316 features 10-MHz bandwidth and  $6\text{-V}/\mu\text{s}$  slew rate with only  $400\text{-}\mu\text{A}$  supply current per channel, providing good ac performance at very-low power consumption. DC applications are well served with a very-low input noise voltage of  $12\text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLVx316 operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are illustrated in the [Typical Characteristics](#) section.

### 8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx316 extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair; see the [Functional Block Diagram](#) section. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.4\text{ V}$  to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.4\text{ V}$ . There is a small transition region, typically  $(V+) - 1.2\text{ V}$  to  $(V+) - 1\text{ V}$ , in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.4\text{ V}$  to  $(V+) - 1.2\text{ V}$  on the low end, up to  $(V+) - 1\text{ V}$  to  $(V+) - 0.8\text{ V}$  on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLVx316 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads of 10 k $\Omega$ , the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see typical characteristic graph [Output Voltage Swing vs Output Current](#) ().

### 8.3.4 Common-Mode Rejection Ratio (CMRR)

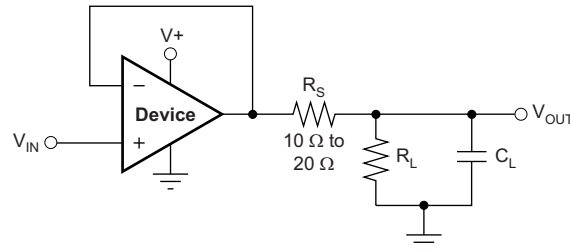
CMRR for the TLVx316 is specified in two ways so the best match for a given application can be selected. First, the [Electrical Characteristics](#) table provides the CMRR of the device in the common-mode range below the transition region [ $V_{\text{CM}} < (V+) - 1.4\text{ V}$ ]. This specification is the best indicator of device capability when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at  $V_{\text{CM}} = -0.2\text{ V}$  to 5.7 V for  $V_{\text{S}} = 5.5\text{ V}$ . This last value includes the variations through the transition region.

### 8.3.5 Capacitive Load and Stability

The TLVx316 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx316 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when the capacitive loading increases. For a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors ( $C_{\text{L}}$  greater than 1  $\mu\text{F}$ ) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See typical characteristic graph, [Small-Signal Overshoot vs Capacitive Load](#) ([Figure 7](#),  $G = -1\text{ V/V}$ ).

## Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically  $10\ \Omega$  to  $20\ \Omega$ ) in series with the output, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.



**Figure 14. Improving Capacitive Load Drive**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset measured at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLVx316 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz ( $-3\ \text{dB}$ ), with a roll-off of 20 dB per decade.

The immunity of an operational amplifier can be accurately measured and quantified over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 12 illustrates the results of this testing on the TLVx316. Detailed information can be found in *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from [www.ti.com](http://www.ti.com).

### 8.3.7 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx316 is approximately 300 ns.

## 8.4 Device Functional Modes

The TLVx316 have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9\ \text{V}$ ) and 5.5 V ( $\pm 2.75\ \text{V}$ ).

## 9 Application and Implementation

### NOTE

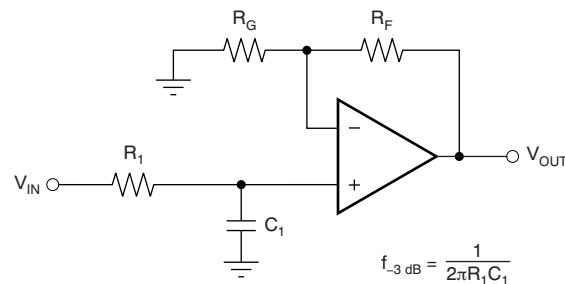
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TLV316, TLV2316, and TLV4316 are powered on when the supply is connected. The devices can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

### 9.2 System Examples

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as shown in [Figure 15](#).

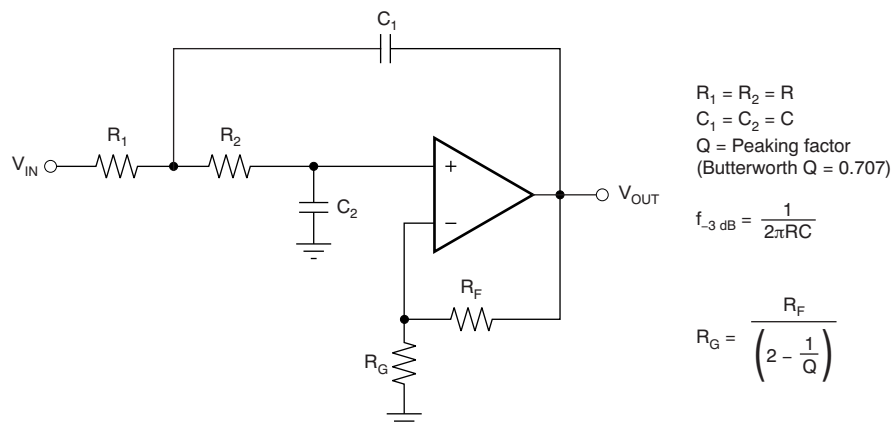


$$f_{-3\text{ dB}} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

**Figure 15. Single-Pole, Low-Pass Filter**

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as shown in [Figure 16](#). For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in a phase shift of the amplifier.



$$\begin{aligned} R_1 &= R_2 = R \\ C_1 &= C_2 = C \\ Q &= \text{Peaking factor} \\ &(\text{Butterworth } Q = 0.707) \end{aligned}$$

$$f_{-3\text{ dB}} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

**Figure 16. Two-Pole, Low-Pass, Sallen-Key Filter**



## 10 Power Supply Recommendations

The TLVx316 is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

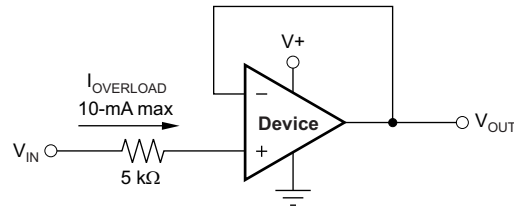
### CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [Layout Guidelines](#).

### 10.1 Input and ESD Protection

The TLVx316 incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 17](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.



**Figure 17. Input Current Protection**

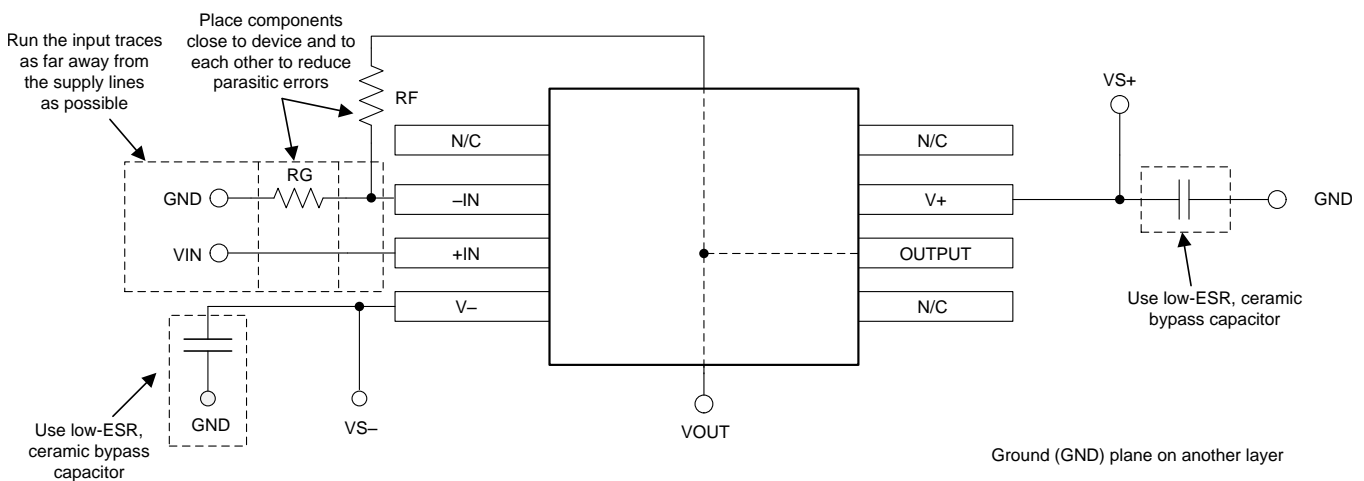
## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see , [Circuit Board Layout Techniques](#) (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example



**Figure 18. Operational Amplifier Board Layout for a Noninverting Configuration**

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

《[TLVx313 面向成本敏感型系统的低功耗、轨到轨输入/输出、500 \$\mu\$ V 典型偏移值、1MHz 运算放大器](#)》（文献编号：SBOS753）。

《[TLVx314 3MHz、低功耗、内部 EMI 滤波器、RRIO、运算放大器](#)》（文献编号：SBOS754）。

《[运算放大器的 EMI 抑制比](#)》（文献编号：SBOA128）。

《[QFN/SON PCB 连接](#)》（文献编号：SLUA271）。

《[四方扁平无引线逻辑器件封装](#)》（文献编号：SCBA017）。

《[电路板布局布线技巧](#)》（文献编号：SLOA089）。

《[单端输入至差分输出转换电路参考设计](#)》（文献编号：TIPD131）。

### 12.2 相关链接

**表 2** 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

**表 2. 相关链接**

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TLV316	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TLV2316	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TLV4316	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2316IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6	<a href="#">Samples</a>
TLV2316IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6	<a href="#">Samples</a>
TLV2316IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2316	<a href="#">Samples</a>
TLV316IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C	<a href="#">Samples</a>
TLV316IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C	<a href="#">Samples</a>
TLV316IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12D	<a href="#">Samples</a>
TLV316IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	12D	<a href="#">Samples</a>
TLV4316IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4316D	<a href="#">Samples</a>
TLV4316IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4316	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2316IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2316IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2316IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV316IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV316IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV316IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV316IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV4316IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4316IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2316IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV2316IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV2316IDR	SOIC	D	8	2500	853.0	449.0	35.0
TLV316IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV316IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV316IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV316IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
TLV4316IDR	SOIC	D	14	2500	333.2	345.9	28.6
TLV4316IPWR	TSSOP	PW	14	2000	853.0	449.0	35.0

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

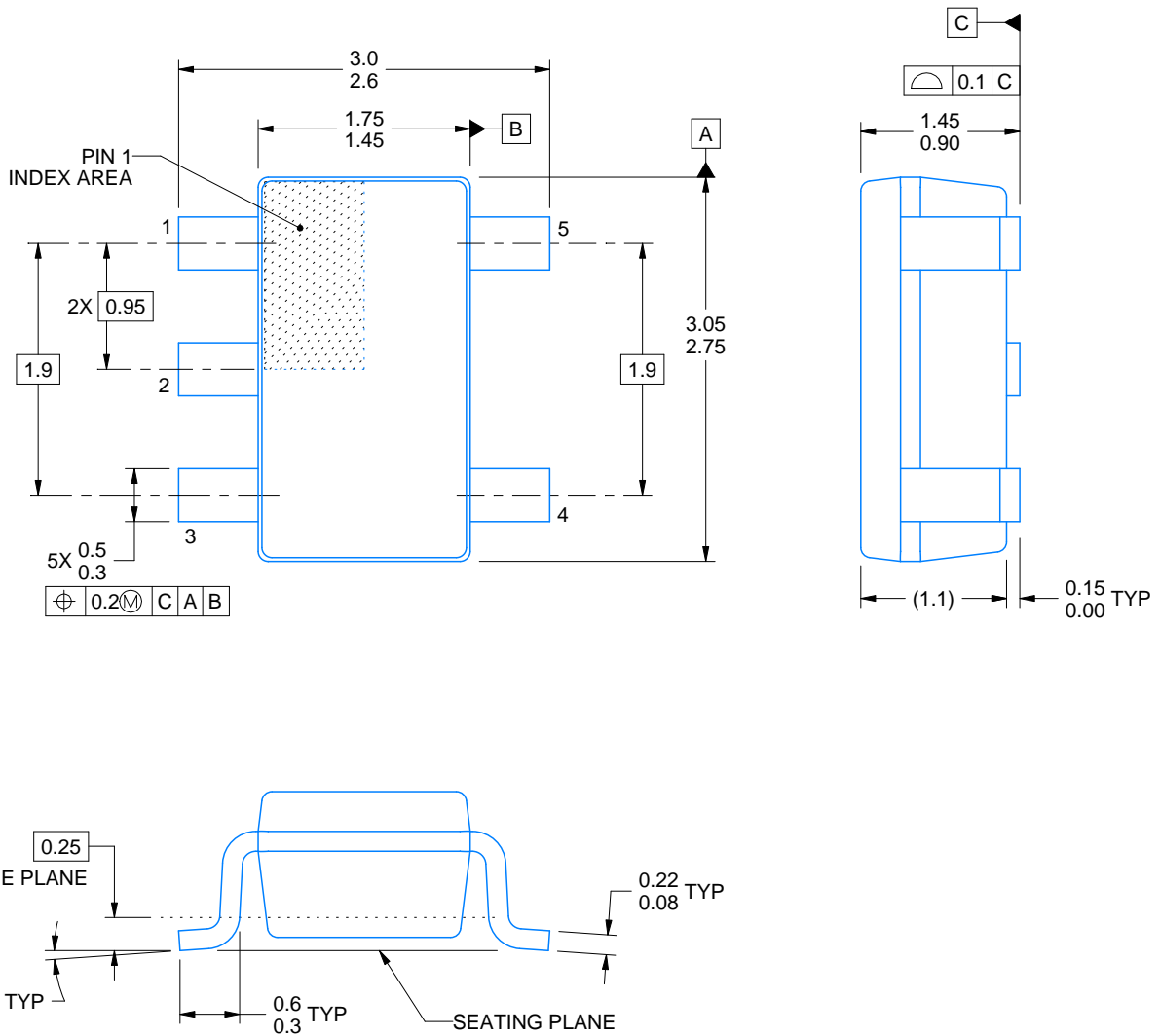
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## 重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司